Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A method for generating a command file of a group of design rule check (DRC) rules for being used by a layout verification tool to verify ~~the~~ a design of an integrated circuit, the method comprising:

(a) selecting a process from a group of processes;

(b) setting a set of parameters; ~~and~~

(c) extracting program codes from a plurality of modules according to the selected process and the set of parameters so as to generate; and

(d) combining the program codes extracted from the plurality of modules to form a corresponding command file of the group of DRC rules to be run by the layout verification tool to verify the design of the integrated circuit.

Claim 2 (currently amended): The method of claim 1 further comprising:

[[(d)]] (e) generating the plurality of modules, the plurality of modules comprising:

a header module comprising program codes for settings of a verification tool of different processes;

a variable module comprising program codes for setting fabrication parameters of different processes;

a layer module comprising program codes for setting layer definitions of different processes; and

an operation module comprising program codes of operation definitions of different processes.

Claim 3 (currently amended): The method of claim 1 wherein the set of parameters ~~comprise~~ comprises number of metal layers.

Claim 4 (currently amended): The method of claim 1 wherein the set of parameters ~~comprise~~ comprises number of poly-silicon layers.

Claim 5 (currently amended): The method of claim 1 wherein the set of parameters ~~comprise~~ comprises package parameters.

Claim 6 (currently amended): A method for generating a command file of a group of layout versus schematic (LVS) rules and layout parasitic extraction (LPE) rules to be used by a layout verification tool to verify ~~the~~ a layout and the parasitic characteristics of an integrated circuit, the method comprising:

(a) selecting a process from a group of processes;

(b) setting a set of parameters; ~~and~~

(c) extracting program codes from a plurality of modules according to the selected process and the set of parameters ~~so as to generate~~ ; and

(d) combining the program codes extracted from the plurality of modules to form a corresponding command file of the group of LVS/LPE rules to be run by the layout verification tool to verify the layout and parasitic characteristics of the integrated circuit.

Claim 7 (currently amended): The method of claim 6 further comprising:

[[(d)]] (e) generating a plurality of modules, the plurality of modules comprising:

a header module comprising program codes for settings of a verification tool of different processes;

a layer module comprising program codes for setting layer definitions of different processes;

an operation module comprising program codes of operation definitions of different processes; and

a device module comprising program codes for declaring devices of different processes.

Claim 8 (currently amended): The method of claim 6 wherein the set of parameters ~~comprise~~ comprises number of metal layers.

Claim 9 (currently amended): The method of claim 6 wherein the set of parameters ~~comprise~~ comprises number of poly-silicon layers.

Claim 10 (currently amended): The method of claim 6 wherein the set of parameters ~~comprise~~ comprises package parameters.

Claim 11 (currently amended): A method for generating a command file of a group of design rule check (DRC) rules or layout versus schematic (LVS) rules and layout parasitic extraction (LPE) rules to be used by a layout verification tool to verify ~~the~~ a layout and ~~the~~ parasitic characteristics of an integrated circuit, the method comprising:

(a) choosing whether to generate a command file of DRC rules or a command file of LVS/LPE rules;

(b) selecting a process from a group of processes;

(c) setting a set of parameters; ~~and~~

(d) extracting program codes from a plurality of modules according to the choice in step [[(k)]] (a), the selected process, and the set of parameters ~~so as to generate~~ a ; and

(e) combining the program codes extracted from a plurality of modules to form the command file of DRC rules or the command file of LVS/LPE rules to be run by the layout verification tool.

Claim 12 (currently amended): The method of claim 11 further comprising:

[[(e)]] (f) generating a plurality of modules, the plurality of modules comprising:

a header module comprising program codes for settings of a verification tool of different processes;

a variable module comprising program codes for setting fabrication parameters of different processes;

a layer module comprising program codes for setting layer definitions of different processes;

an operation module comprising program codes of operation definitions of different processes; and

a device module comprising program codes for declaring devices of different processes[[;]] .

Claim 13 (currently amended): The method of claim 11 wherein the set of parameters ~~comprise~~ comprises number of metal layers.

Claim 14 (currently amended): The method of claim 11 wherein the set of parameters ~~comprise~~ comprises number of poly-silicon layers.

Claim 15 (currently amended): The method of claim 11 wherein the set of parameters ~~comprise~~ comprises package parameters.